



Influence of Temperature on Microelectronics and System Reliability: A Physics of Failure Approach (Electronic Packaging)

Pradeep Lall, Michael Pecht, Edward B. Hakim

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This book raises the level of understanding of thermal design criteria. It provides the design team with sufficient knowledge to help them evaluate device architecture trade-offs and the effects of operating temperatures. The author provides readers a sound scientific basis for system operation at realistic steady state temperatures without reliability penalties. Higher temperature performance than is commonly recommended is shown to be cost effective in production for life cycle costs.

The microelectronic package considered in the book is assumed to consist of a semiconductor device with first-level interconnects that may be wirebonds, flip-chip, or tape automated bonds; die attach; substrate; substrate attach; case; lid; lid seal; and lead seal. The temperature effects on electrical parameters of both bipolar and MOSFET devices are discussed, and models quantifying the temperature effects on package elements are identified. Temperature-related models have been used to derive derating criteria for determining the maximum and minimum allowable temperature stresses for a given microelectronic package architecture.

The first chapter outlines problems with some of the current modeling strategies. The next two chapters present microelectronic device failure mechanisms in terms of their dependence on steady state temperature, temperature cycle, temperature gradient, and rate of change of temperature at the chip and package level. Physics-of-failure based models used to characterize these failure mechanisms are identified and the variabilities in temperature dependence of each of the failure mechanisms are characterized. Chapters 4 and 5 describe the effects of temperature on the performance characteristics of MOS and bipolar devices. Chapter 6 discusses using high-temperature stress screens, including burn-in, for high-reliability applications. The burn-in conditions used by some manufacturers are examined and a physics-of-failure approach is described. The final chapter overviews existing guidelines for thermal derating of microelectronic devices, which presently involve lowering the junction temperature. The reader then learns how to use physics-of-failure models presented in the previous chapters for various failure processes, to evaluate the sensitivity of device life to variations in manufacturing defects, device architecture, temperature, and non-temperature stresses.



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